

GENERAL DESCRIPTION

PT-40G-SR-BD is a four-channel, LC Duplex, Fiber Optic QSFP+ transceiver for 40 Gigabit Ethernet applications. This transceiver is a high performance module for short-range duplex data communication. It integrates four electrical data lanes in each direction into transmission over a single LC duplex fiber optic cable. Each electrical lane operates at 10.3125 Gbps and conforms to the 40GE XLPPI interface.

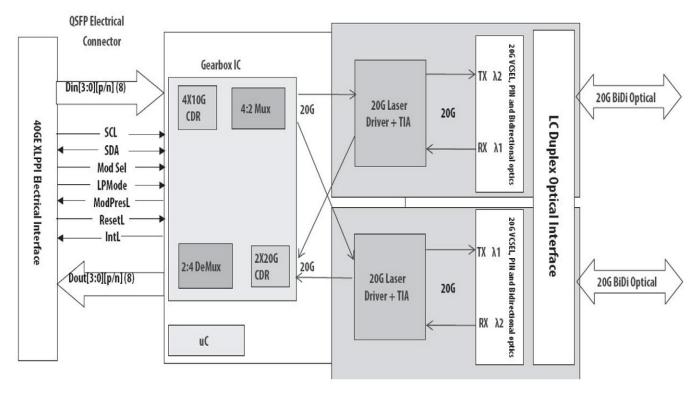
The transceiver internally multiplexes an XLPPI 4x10G interface into two 20Gb/s electrical channels, transmitting and receiving each optically over one simplex LC fiber using bi-directional optics. This results in an aggregate bandwidth of 40 Gbps into a duplex LC cable. This allows reuse of the installed LC duplex cabling infrastructure for 40 GbE application. Link distances up to 100 m using OM3 and 150 m using OM4 optical fiber are supported. These modules are designed to operate over multi-mode fiber systems using a nominal wavelength of 850 nm on one end and 900 nm on the other end. The electrical interface uses a 38 contact QSFP+ type edge connector. The optical interface uses a conventional LC duplex connector.

PRODUCT FEATURES

- Compliant with the 40 GbE XLPPI electrical specification per IEEE 802.3ba-2010
- Compliant with QSFP+ SFF-8436 Specification
- Aggregate bandwidth of 40 Gbps
- Operates at 10.3125 Gbps per electrical channel with 64b/66b encoded data
- OSFP MSA compliant
- Capable of up to 100 m reach over OM3 Multi-Mode Fiber (MMF) and reach over 150 m over OM4 MMF
- Single +3.3V power supply
- Built-in digital diagnostic functions
- Temperature range 0°C to 70°C
- RoHS compliant
- Utilizes a standard LC duplex fiber cable allowing reuse of existing cable infrastructure

APPLICATIONS

- 40 Gigabit Ethernet interconnects
- Datacom/Telecom switch & router connections
- Data aggregation and backplane applications
- Proprietary protocol and density applications



Transceiver block diagram

ABSOLUTE MAXIMUM RATINGS

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_s	-40	+85	°C
Power Supply Voltage	V _{cc} T, R	-0.5	4	V
Relative Humidity (non-condensing)	RH	0	85	%

RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min	Typical	Max	Unit	Note
Case Operating Temperature	T _c	0		+70	°C	
Supply Voltage	V _{CC} T, R	+3.13	3.3	+3.47	V	
Supply Current	I _{cc}			1000	mA	
Power Dissipation	PD			3.5	W	

ELECTRICAL CHARACTERISTICS

TOP = 0 *TO* 70 °C, *VCC* = 3.13 *TO* 3.47 *VOLTS*

Parameter	Symbol	Min	Typical	Max	Unit	Note
Data Rate per Channel			10.3125	11.2	Gbps	
Power Consumption			2.5	3.5	W	
Supply Current	lcc		0.75	1.0	А	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			150	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	
		Transmitt	er			
Single Ended Output Voltage Tolerance		0.3		4	V	1
Common mode Voltage Tolerance		15			mV	
Transmit Input Diff Voltage	VI	120		1200	mV	
Transmit Input Diff Impedance	ZIN	80	100	120		
Data Dependent Input Jitter	DDJ			0.1	UI	
Data Input Total Jitter	TJ			0.28	UI	
		Receive	r			
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	Vo		600	800	mV	
Rx Output Rise and Fall Voltage	Tr/Tf			35	ps	1
Total Jitter	TJ			0.7	UI	
Deterministic Jitter	DJ			0.42	UI	

Note 1: 20~80%

OPTICAL PARAMETERS

TOP = 0 *TO 70* °C, *VCC* = 3.0 *TO 3.6 VOLTS*

Symbol	Min	Typical	Max	Unit	Note
Trans	mitter				
λ	832	850	868	nm	
λ	882	900	918	nm	
Pm		0.5	0.65	nm	
Pavg	-4	-2.5	+5.0	dBm	
Poff			-30	dBm	
ER	3.5			dB	
Rin			-128	dB/HZ	1
			12	dB	
Rec	eiver				
λ	882	900	918	nm	
λ	832	850	868	nm	
R		-6		dBm	
P _{MAX}	+3			dBm	
P_{Min}	+7				
Rrx			-12	dB	
LOSD			-14	dBm	
LOSA	-30			dBm	
LOSH	0.5			dB	
	Trans λ λ Pm Pavg Poff ER Rin Rec λ λ R P _{MAX} P _{Min} Rrx LOSD LOSA	Transmitter λ 832 λ 882 Pm -4 Poff ER ER 3.5 Rin -4 Receiver λ 882 λ 832 R P _{MAX} +3 P _{Min} +7 Rrx LOSD LOSA -30	Transmitter λ 832 850 λ 882 900 Pm 0.5 Pavg -4 -2.5 Poff ER 3.5 Rin -8 -8 R -6 -6 P _{MAX} +3 -4 P _{Min} +7 -7 Rx LOSD LOSA -30	Transmitter λ 832 850 868 λ 882 900 918 Pm 0.5 0.65 Pavg -4 -2.5 +5.0 Poff -30 ER 3.5 Rin -128 Receiver λ 882 900 918 λ 832 850 868 R -6 -6 P _{MAX} +3 -7 Rrx -12 -12 LOSD -14 -14 LOSA -30 -30	Transmitter λ 832 850 868 nm λ 882 900 918 nm Pm 0.5 0.65 nm Pavg -4 -2.5 +5.0 dBm Poff -30 dBm ER 3.5 dB dB/HZ Rin -128 dB/HZ λ 882 900 918 nm λ 832 850 868 nm R -6 dBm dBm P _{MAX} +3 dBm dBm P _{MIn} +7 -12 dB LOSD -14 dBm LOSA -30 dBm dBm

Note 1: 12dB reflection.

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all QSFP+ SRBD. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in flowing. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Byte Address	Description	Туре
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85 Reserved (4 Bytes)		Read Only
86-97 Control (12 Bytes)		Read/Write
98-99 Reserved (2 Bytes)		Read/Write
100-106 Module and Channel Masks (7 Bytes)		Read/Write
107-118 Reserved (12 Bytes)		Read/Write
119-122 Reserved (4 Bytes)		Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Byte Address Description		Туре
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225 Reserved (2 Bytes)		Read Only
226-239 Reserved (14 Bytes)		Read/Write
240-241 Channel Controls (2 Bytes)		Read/Write
242-253 Reserved (12 Bytes)		Read/Write
254-255 Reserved (2 Bytes)		Read/Write

2-wire serial address, 1010000x (A0h)" (3 Bytes) ID and status (19 Bytes) Interrupt Flags 21 (12 Bytes) Module Monitors 33 (48 Bytes) Channel Monitors 81 (4 Bytes) Reserved 85 (12 Bytes) Control 97 (2 Bytes) Reserved 99 Module and Channel Mask (7 Bytes) 106 (12 Bytes) Reserved 118 Password Change Entry (4 Bytes) Area (Optional) 122 Password Entry Area (4 Bytes) (Optional) 126 (1 Bytes) Page Select Byte 127 Page 00 Page 02 (Optional) Page 03 128 (64 Bytes) 128 (128 Bytes) 128 (48 Bytes) Base ID Fields User EEPROM Data Module Threshold 191 175 (32 Bytes) (48 Bytes) Extended ID Channel Threshold 223 223 (32 Bytes) (2 Bytes) Vendor Specific ID Reserved 225 Vendor Specific Channel (16 Bytes) Controls 24 (12 Bytes) Channel Monitor Masks 253 (2 Bytes) Reserved

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 µm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 µm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125µm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand [†]
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tof. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

TIMING FOR SOFT CONTROL AND STATUS FUNCTIONS

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on [1], hot plug or rising edge of Reset until the module is fully functional [2].
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on [1] until module responds to data transmission over the 2-wire serial bus.
Monitor Data Ready Time	t_data	2000	ms	Time from power on [1] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted.
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional [2].
LPMode Assert Time	ton_ LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode=Vih) until module power consumption enters lower Power Level.
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol.
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read [3] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted.
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted.
Mask Assert Time	ton_mask	100	ms	Time from mask bit set [4] until associated IntL assertion is inhibited.
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared [4] until associated IntlL operation resumes.
ModSelL Assert Time	ton_ ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus.
ModSelL Deassert Time	toff_ ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus.
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set [4] until module power consumption enters lower Power Level.
Power_over-ride or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared [4] until the module is fully functional [3].

Note 1: Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.

Note 2: Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.

Note 3: Measured from falling clock edge after stop bit of read transaction.

Note 4: Measured from falling clock edge after stop bit of write transaction.

PIN ASSIGNMENT

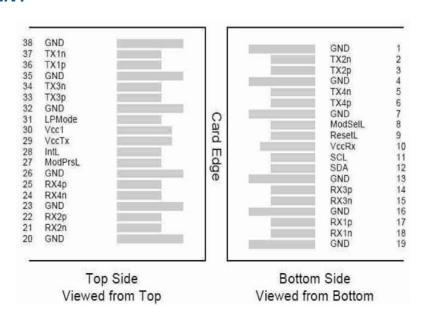


Diagram of host board connector block pin numbers and name

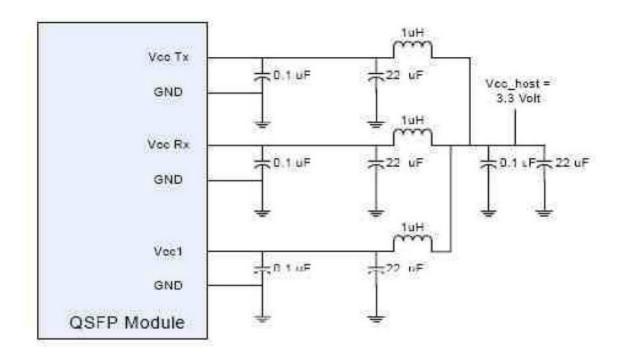
PIN DESCRIPTION

Pin	Logic	Symbol	Name / Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Тх4р	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3 V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply Transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Тх3р	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

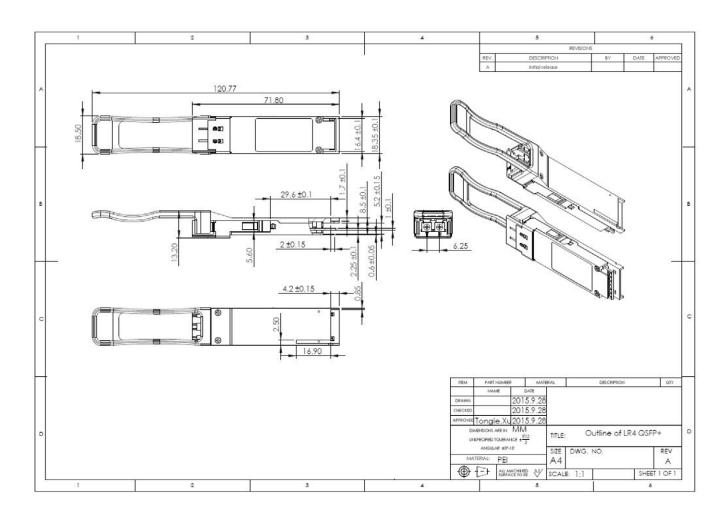
Notes:

- 1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
- 2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

RECOMMENDED CIRCUIT



MECHANICAL DIMENSIONS



ORDERING INFORMATION

PT-40G-SR-BD

Part Number	Product Description

40GBASE-SR BIDI QSFP+