

PT-400G-DR4DD-31

DATASHEET



400 Gb/s QSFP-DD DR4 500 m Transceiver Hot Pluggable
MTP/MPO-12 Connector
Single-Mode 4 x 100 Gb/s EML 1310 nm transmitter

PRODUCT FEATURES

400GBASE-DR4 QSFP-DD Module

- ▶ 4 parallel EML 1310 nm design
- ▶ MTP/MPO-12 connector
- ▶ Compliant to QSFP-DD MSA
- ▶ IEEE 802.3cd 400GBASE-DR4 specification compliant
- ▶ Compliant with CMIS 4.0 management interface specifications
- ▶ 4 x 106.25 Gb/s electrical interface (400GAUI-8)
- ▶ Up to 500 m transmission on single-mode fiber (SMF) with FEC
- ▶ Maximum power consumption: 10 W
- ▶ Single +3.3 V power supply operating
- ▶ Temperature range: 0°C to 70°C
- ▶ RoHS compliant

APPLICATIONS

- ▶ Networks
- ▶ Data center and Cloud

GENERAL DESCRIPTION

The PT-400G-DR4DD-31 is a 400 Gb/s QSFP-DD DR4 optical module designed for 500 m optical communication applications. The module converts 8 channels of 50 Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100 Gb/s operation for an aggregate data rate of 400 Gb/s.

On the receiver side, the module converts 4 channels of parallel optical signals of 100 Gb/s each channel for an aggregate data rate of 400 Gb/s into 8 channels of 50 Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP-DD DR4 module receptacle. Host FEC is required to support up to 500 m fiber transmission.

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|------------------------------------|--------------|------|-----|------|
| Storage Temperature | T_s | -40 | +85 | °C |
| Supply Voltage | $V_{cc,T,R}$ | -0.5 | 4 | V |
| Relative Humidity (non-condensing) | RH | 10 | 95 | % |

RECOMMENDED OPERATING ENVIRONMENT

| Parameter | Symbol | Min | Typical | Max | Unit |
|----------------------------|--------------|-------|---------|----------------------|------|
| Case Operating Temperature | T_c | 0 | | +70 | °C |
| Supply Voltage | $V_{cc,T,R}$ | +3.13 | 3.3 | +3.47 | V |
| Supply Current | I_{cc} | | | 3000 | mA |
| Power Dissipation | PD | | | 10 | W |
| Pre-FEC Bit Error Ratio | | | | 2.4×10^{-4} | |
| Link Distance over OM4 | | | | 500 | m |

ELECTRICAL CHARACTERISTICS

$T_{OP} = 0 \text{ to } 70 \text{ } ^\circ\text{C}$, $V_{cc} = 3.13 \text{ to } 3.47 \text{ V}$

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|--|-----------|--------------|---------|-----|------|--------|
| Data Rate per Channel | | | 26.5625 | | Gbps | |
| Differential termination mismatch | | | | 10 | % | |
| Transmitter | | | | | | |
| Single Ended Output Voltage Tolerance | | 0.3 | | 4 | V | |
| Transmit Input Diff Voltage | V_I | 900 | | | mV | |
| Common Mode to Differential Return Loss min | | 802.3ck 120G | | | dB | |
| Receiver | | | | | | |
| Single Ended Output Voltage Tolerance | | 0.3 | | 4 | V | |
| Rx Output Diff Voltage | V_o | | | 900 | mV | |
| Near-end ESMW (eye symmetry mask width) | | | TBD | | | |
| Near-end eye height, differential | | 24 | | | mV | |
| Near-end vertical eye closure | | | | 7.5 | dB | |
| Far-end ESMW (eye symmetry mask width) | | | TBD | | | |
| Far-end eye height, differential | | 24 | | | mV | |
| Far-end vertical eye closure | | | | 7.5 | dB | |
| Far-end pre-cursor ISI ratio | | TBD | | | | |
| Common Mode to Differential Conversion Return Loss | | 802.3ck 120G | | | dB | |
| Rx Output Rise and Fall Voltage | T_r/T_f | | TBD | | ps | 20~80% |

OPTICAL PARAMETERS

$T_{OP} = 0 \text{ to } 70 \text{ } ^\circ\text{C}$, $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|------------------|--------|---------|--------|-------|------------------|
| Transmitter | | | | | | |
| Modulation Format | | PAM4 | | | | |
| Data Rate per Channel | | | 53.125 | | Gbps | |
| Lane Wavelength Range | | 1304.5 | 1310 | 1317.5 | nm | |
| Average Optical Power each lane | Po | -2.9 | | 4.0 | dBm | |
| RMS Spectral Width | | | | 0.6 | nm | |
| Optical Modulation Amplitude (OMA), each lane | | -0.8 | | 4.2 | dBm | |
| Launch Power in OMAouter minus TDECQ, each lane | | -2.2 | | 3.5 | dBm | |
| Extinction Ratio | ER | 3.5 | | | dB | |
| Transmitter Transition Time, Each lane | | | | 17 | ps | |
| Average Launch Power OFF Transmitter, each lane | Poff | | | -30 | dBm | |
| Relative Intensity Noise | Rin | | | -136 | dB/HZ | 12 dB reflection |
| Optical Return Loss Tolerance | | | | 21 | dB | |
| Transmitter Reflectance | | | | -26 | dBm | |
| Receiver | | | | | | |
| Modulation Format | | PAM4 | | | | |
| Data Rate per Channel | | | 53.125 | | Gbps | |
| Lane Wavelength Range | | 1304.5 | 1310 | 1317.5 | nm | |
| Damage Threshold | THd | 5 | | | dBm | 12 dB reflection |
| Average Receive Power, each lane | R | -5.9 | | 4 | dBm | |
| Receiver Power (OMA), each lane | RxOMA | | | 4.2 | dBm | |
| Stressed eye closure for PAM4 (SECQ), lane under test | | | 4.5 | | dB | |
| Stressed Receiver Sensitivity (OMA) per lane | SRS | | | -1.9 | dBm | |
| RSSI Accuracy | | -2.5 | | 2.5 | dB | |
| Receiver Reflectance | Rrx | | | -26 | dB | |
| LOS De-Assert | LOS _D | | | -10 | dBm | |
| LOS Assert | LOS _A | -20 | | | dBm | |
| LOS Hysteresis | LOS _H | 1.5 | | | dB | |

PIN ASSIGNMENT

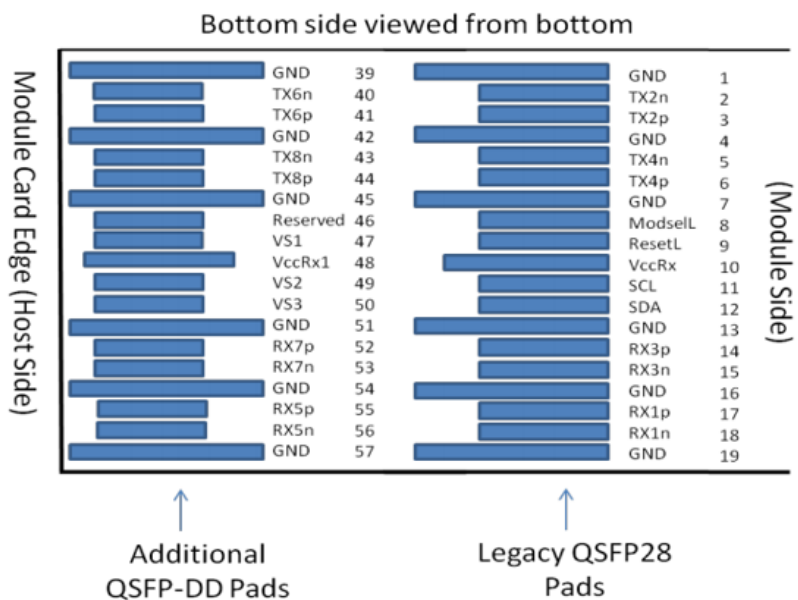
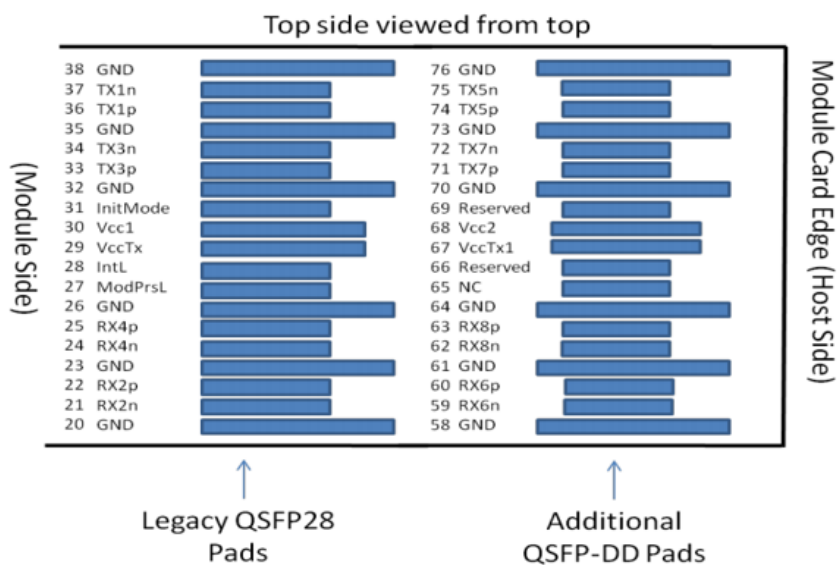


Diagram of Host Board Connector Block Pin Numbers and Name

PIN DESCRIPTION

| Pin | Logic | Symbol | Definition | Note |
|-----|------------|--------------|-------------------------------------|------|
| 1 | | GND | Ground | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | |
| 4 | | GND | Ground | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | |
| 7 | | GND | Ground | 1 |
| 8 | LVTTTL-I | ModSelL | Module Select | |
| 9 | LVTTTL-I | ResetL | Module Reset | |
| 10 | | VccRx | +3.3 V Power Supply Receiver | 2 |
| 11 | LVCMOS-I/O | SCL | 2-Wire Serial Interface Clock | |
| 12 | LVCMOS-I/O | SDA | 2-Wire Serial Interface Data | |
| 13 | | GND | Ground | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | |
| 16 | | GND | Ground | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | |
| 19 | | GND | Ground | 1 |
| 20 | | GND | Ground | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | |
| 23 | | GND | Ground | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | |
| 26 | | GND | Ground | 1 |
| 27 | LVTTTL-O | ModPrsL | Module Present | |
| 28 | LVTTTL-O | IntL/RxLOS | Interrupt/optional RxLOS | |
| 29 | | VccTx | +3.3 V Power Supply Transmitter | 2 |
| 30 | | Vcc1 | +3.3 V Power Supply | 2 |
| 31 | LVTTTL-I | LPMoDe/TxDis | Low Power mode/optional TX Disable | |
| 32 | | GND | Ground | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | |
| 35 | | GND | Ground | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | |
| 38 | | GND | Ground | 1 |

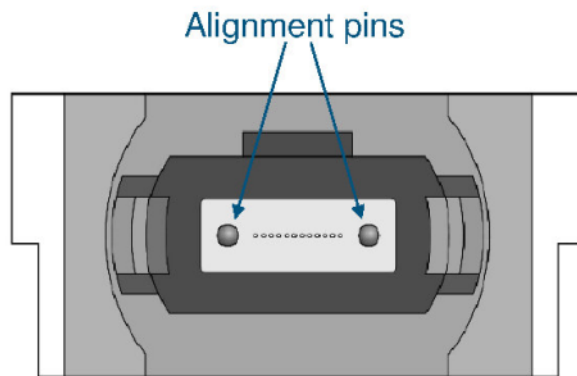
PIN DESCRIPTION (cont.)

| Pin | Logic | Symbol | Definition | Note |
|------------|---------------|---------------|---|-------------|
| 39 | | GND | Ground | 1 |
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input | |
| 41 | CML-I | Tx6p | Transmitter Non-Inverted Data Input | |
| 42 | | GND | Ground | 1 |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input | |
| 44 | CML-I | Tx8p | Transmitter Non-Inverted Data Input | |
| 45 | | GND | Ground | 1 |
| 46 | LVC MOS/CML-I | P/VS4 | Programmable/Module Vendor Specific 4 | 5 |
| 47 | LVC MOS/CML-I | P/VS1 | Programmable/Module Vendor Specific 1 | 5 |
| 48 | | VccRx1 | 3.3 V Power Supply | 2 |
| 49 | LVC MOS/CML-O | P/VS2 | Programmable/Module Vendor Specific 2 | 5 |
| 50 | LVC MOS/CML-O | P/VS3 | Programmable/Module Vendor Specific 3 | 5 |
| 51 | | GND | Ground | 1 |
| 52 | CML-O | Rx7p | Receiver Non-Inverted Data Output | |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output | |
| 54 | | GND | Ground | 1 |
| 55 | CML-O | Rx5p | Receiver Non-Inverted Data Output | |
| 56 | CML-O | Rx5n | Receiver Inverted Data Output | |
| 57 | | GND | Ground | 1 |
| 58 | | GND | Ground | 1 |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output | |
| 60 | CML-O | Rx6p | Receiver Non-Inverted Data Output | |
| 61 | | GND | Ground | 1 |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output | |
| 63 | CML-O | Rx8p | Receiver Non-Inverted Data Output | |
| 64 | | GND | Ground | 1 |
| 65 | | NC | Not connected | 3 |
| 66 | | Reserved | | 3 |
| 67 | | VccTx1 | 3.3 V Power Supply | 2 |
| 68 | | Vcc2 | 3.3 V Power Supply | 2 |
| 69 | LVC MOS-I | ePPS/Clock | 1PPS PTP clock or reference clock input | |
| 70 | | GND | Ground | 1 |
| 71 | CML-I | Tx7p | Transmitter Non-Inverted Data Input | |
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input | |
| 73 | | GND | Ground | 1 |
| 74 | CML-I | Tx5p | Transmitter Non-Inverted Data Input | |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input | |
| 76 | | GND | Ground | 1 |

Notes:

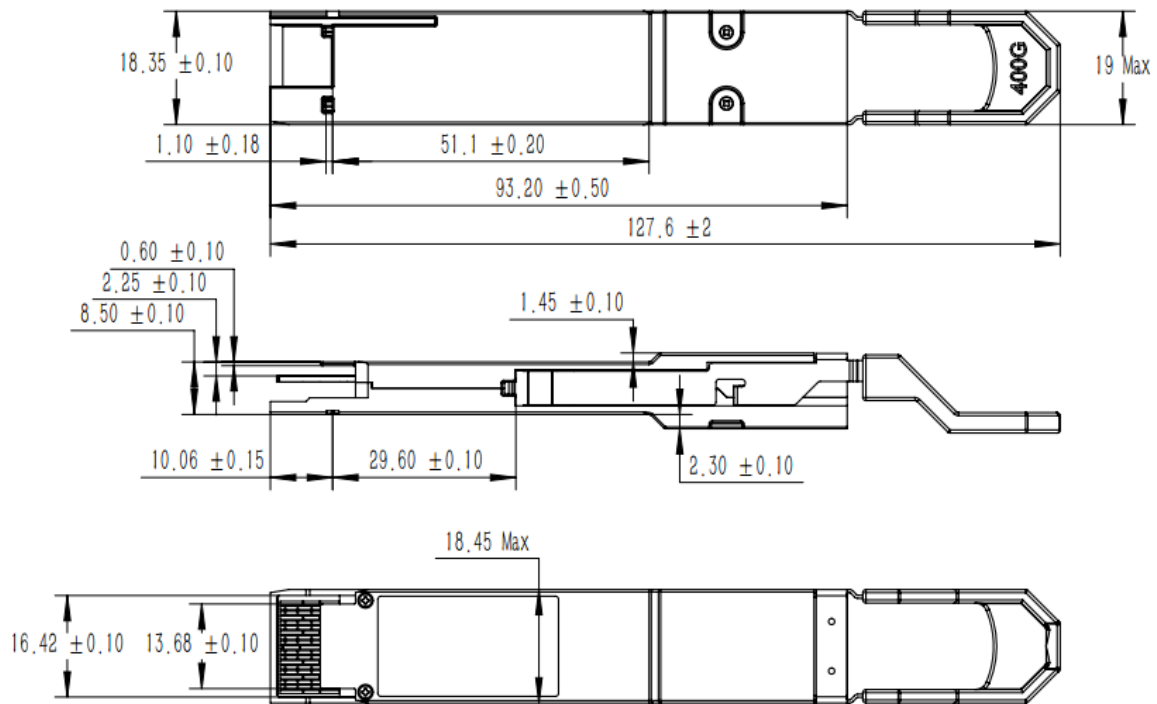
1. GND is the symbol for single and supply (power) common for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500 mA.
3. Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure 2 for pad locations). Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.
5. Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.

OPTICAL INTERFACE



Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

MECHANICAL DIMENSIONS



ORDERING INFORMATION

| Part Number | Description | Application | Data Rate | Laser Source | Fiber Type |
|------------------|------------------|--------------|---------------|--------------|-------------------|
| PT-400G-DR4DD-31 | 400G DR4 QSFP-DD | 400GBASE-DR4 | 400G Ethernet | EML | Single-Mode Fiber |