PT-400G-DR4112-31

DATASHEET

400 Gb/s QSFP112 DR4 500 m Transceiver Hot Pluggable
MTP/MPO-12 Connector
Single-Mode 4 x 100 Gb/s EML 1310 nm transmitter

PRODUCT FEATURES

400GBASE-DR4 QSFP112 Module

- QSFP112 MSA compliant
- 4 x 106.25 Gb/s PAM4 electrical interface (400GAUI-4)
- Maximum power consumption: 9W
- MPO-12-APC connector
- Up to 500 m transmission on single-mode fiber
- Operating case temperature: 0°C~70°C
- Single 3.3 V power supply
- RoHS-6 compliant

APPLICATIONS

- 400G Ethernet
- Data Center Applications

COMPLIANCE

- QSFP112 MSA Rev2.1
- IEEE 802.3cn
- IEEE 802.3ck
- CMIS Rev5.2
- RoHS compliance
- GR-468-CORE

GENERAL DESCRIPTION

The PT-400G-DR4112-31 transceiver is a high-performance, cost-effective module for optical data communication applications supporting 400G Ethernet. The PT-400G-DR4112-31 is designed to operate in switch and router applications supporting QSFP112 MSA / 400G DR4 compliant traffic for links up to 500 m.

The PT-400G-DR4112-31 can convert 4-channel 106.25 Gb/s electrical data to 4-channel 106.25 Gb/s optical signals. Similarly, it optically converts 4-channel 106.25 Gb/s optical signals to 4-channel electrical data output on the receiver side. It has been designed to withstand the maximum range of external operating conditions including temperature, humidity and EMI. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typical	Max	Unit
Storage Temperature	TSTG	-40		85	ºC
Operating Relative Humidity (non-condensing)	RH	5		85	%
Supply Voltage	VCC	-0.5	3.3	3.6	V
Optical Input Power	PIN			5	dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typical	Max	Unit
Case Temperature	Tcase	0		70	ºC
Supply Voltage	VCC	3.135	3.3	3.465	V
Supply Current	ICC			2871	mA
Module Power Dissipation	P			9	W

ELECTRICAL AND OPTICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter						
Optical data rate, each lane		53.125±100ppm			GBd	
Modulation format		PAM4				
Line wavelengths	λ	1304.5	1311	1317.5	nm	
Average launch power, each lane	P_{AVG}	-2.9		4	dBm	
Optical Modulation Amplitude (OMA), each lane	OMA	-0.8		4.2	dBm	
Extinction ratio	ER	3.5			dB	
Side-mode suppression ratio	SMSR	30			dB	
Launch power in OMA minus TDECQ, each lane		-2.2			dBm	
Transmitter and Dispersion Eye Closure for PAM4, each lane	TDECQ			3.4	dB	
Optical return loss tolerance				21.4	dB	
Transmitter reflectance				-26	dB	
Average launch power of OFF transmitter, each lane				-15	dBm	
Electrical data rate, each lane		53.125±100ppm			GBd	
Differential pk-pk input voltage tolerance	Vpp	800			mV	
DC common-mode voltage	Vcm	-350		2850	mV	1
Differential termination resistance mismatch		-10		10	%	
Effective return loss				8.5	dB	
Differential to common-mode input return loss		IEEE 802.3ck Equation (120G-2)			dB	
Module stressed input test		IEEE 802.3ck 120G.3.4.2				2

Notes:

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

2. BER specified in IEEE 802.3ck 120G.1.1.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Receiver						
Optical data rate, each lane		53.125±100ppm			GBd	
Modulation format		PAM4				
Damage threshold, each lane		5			dBm	
Line wavelengths	λ	1304.5	1311	1317.5	nm	
Average receiver power, each lane		-5.9		4	dBm	
Receiver power, each lane (OMA)				4.2	dBm	
Receiver sensitivity (OMAouter), each lane				-4.4	dBm	
Stressed receiver sensitivity (OMAouter), each lane (max)				-1.9	dBm	
Receiver reflectance				-26	dB	
Electrical data rate, each lane		53.125±100ppm			GBd	
Differential termination resistance mismatch		-10		10	%	
Differential output voltage pk-pk	Vpp			845	mV	
DC common-mode voltage	Vcm	-350		2850	mV	1
Effective return loss		8.5			dB	
Common to differential mode conversion return loss		IEEE 802.3ck Equation (120G-1)			dB	

Note:

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

DIGITAL DIAGNOSTIC FUNCTIONS

Parameter	Symbol	Min	Typical	Max	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3		3	°C	1
Supply voltage monitor absolute error	DMI_Vcc	-3%		3%	V	2
Bias current monitor absolute error	DMI_Ibias	-10%		10%	mA	
Laser power monitor absolute error	DMI_Tx	-3		3	dB	
RX power monitor absolute error	DMI_Rx	-3		3	dB	

Notes:

1. Temperature here is depending on module case around Max power dissipation. Temperature monitor is done over operating temperature.

2. Supply voltage monitor is done over operating voltage.

CONTROL AND STATUS I/O TIMING CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Unit	Note
MgmtInitDuration	Max MgmtInit Duration			2000	ms	1
ResetL Assert Time	t_reset_init	10			μs	2
IntL Assert Time	ton_IntL			200	ms	3
IntL Deassert Time	toff_IntL			500	μs	4
Rx LOS Assert Time	ton_los			100	ms	5
Flag Assert Time	ton_flag			200	ms	6
Mask Assert Time	ton_mask			100	ms	7
Mask Deassert Time	toff_mask			100	ms	8

Notes:

1. Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.
2. Minimum pulse time on the ResetL signal to initiate a module reset.
3. Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
4. Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
5. Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
6. Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
7. Time from mask bit set (value=1b) until associated IntL assertion is inhibited.
8. Time from mask bit cleared (value=0b) until associated IntL operation resumes.

SURGE CURRENT REQUIREMENTS

Parameter	Symbol	Min	Typical	Max	Unit	Note
VCC			3.3		V	
Vcc set point accuracy		-5		5	%	
Power Supply Noise including ripple				50	mV	
Module Maximum Current Inrush with LPMode Pin asserted				0.55	A	
Module Maximum Current Inrush with LPMode Pin deasserted				1.3	A	
Module Current Ramp Rate				100	mA/us	
High Power Mode Power Class 8 module						
Power Consumption	P_8			9	W	
Instantaneous peak current	Icc_ip_8			3600	mA	
Sustained peak current	Icc_sp_8			2970	mA	
Steady state current	Icc_8			2871	mA	1

Note:

1. The module must stay within its declared power class.

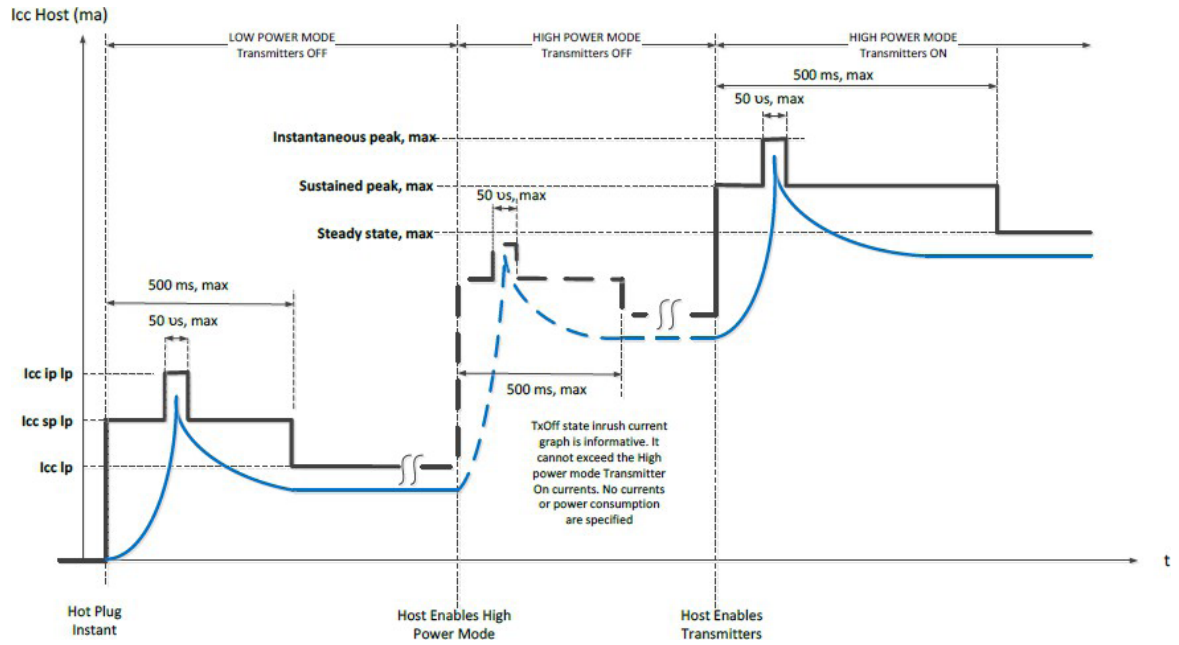

Figure 1

PIN-OUT DEFINITIONS

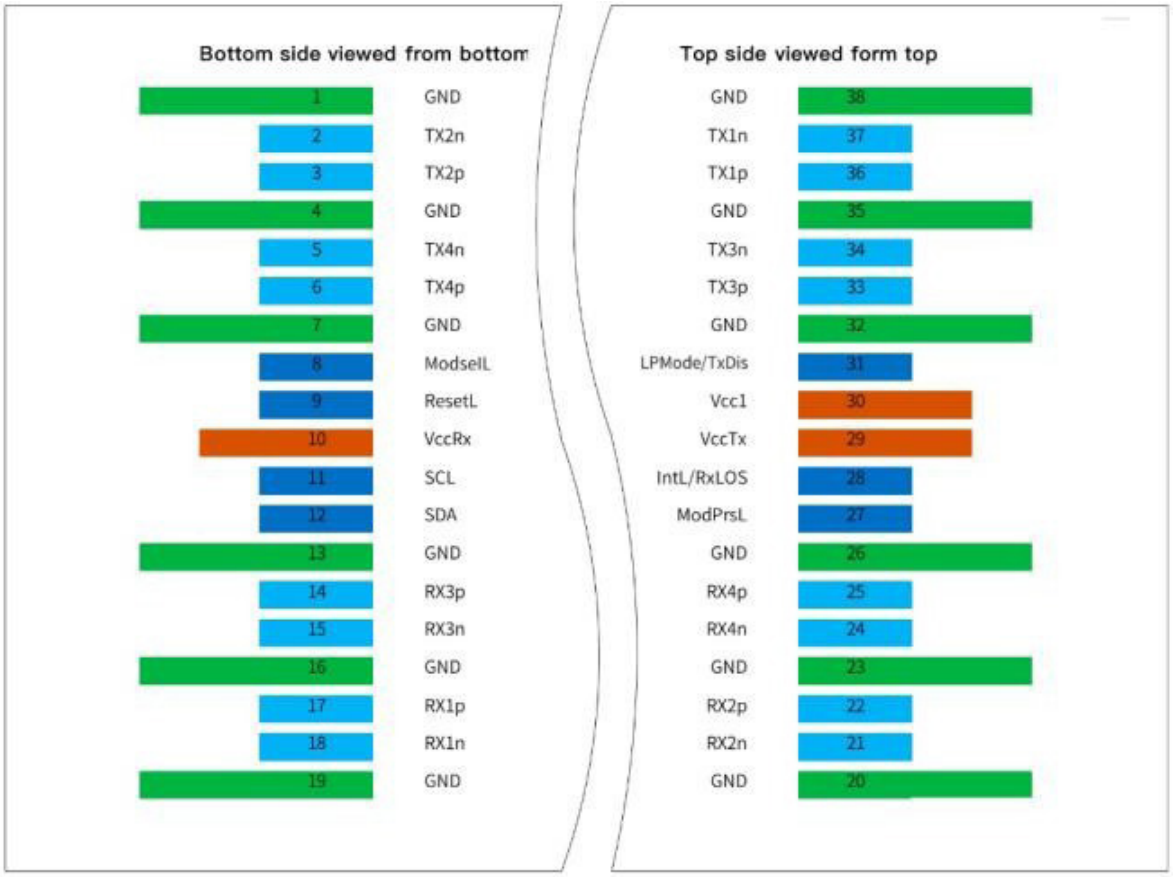

Figure 2

PIN FUNCTION DEFINITIONS

Pin	Logic	Symbol	Description	Plug Sequence	Note
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-I	ModPrsL	Module Present	3B	
28	LVTTL-I	IntL/RxLOS	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3 V Power Supply Transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

Requirements, defined for the host side of the Host Edge Card Connector, are listed in the "Electrical and Optical Characteristics" table. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

BLOCK DIAGRAM OF TRANSCEIVER

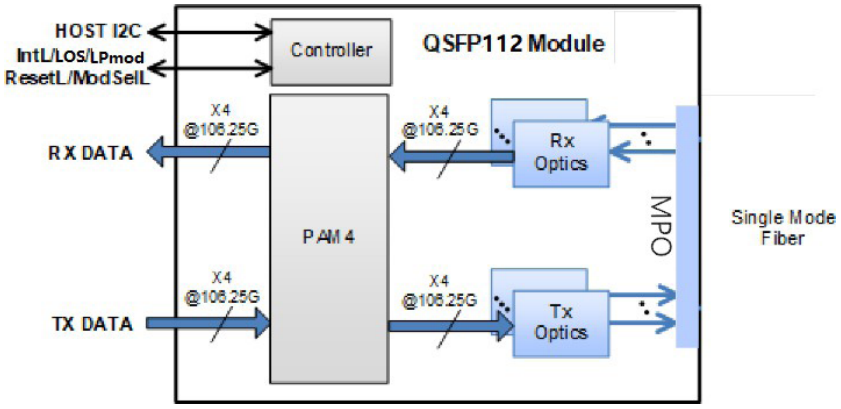

Figure 3

<Transmitter Section>: Converts 4-channel 106.25Gb/s electrical data to 4-channel 1310nm 106.25Gb/s optical signals for 425Gb/s optical transmission.

<Receiver Section>: Similarly, it optically converts 4-channel 1310nm 106.25Gb/s optical signals to 4-channel electrical data output on the receiver side.

RECOMMENDED INTERFACE CIRCUIT

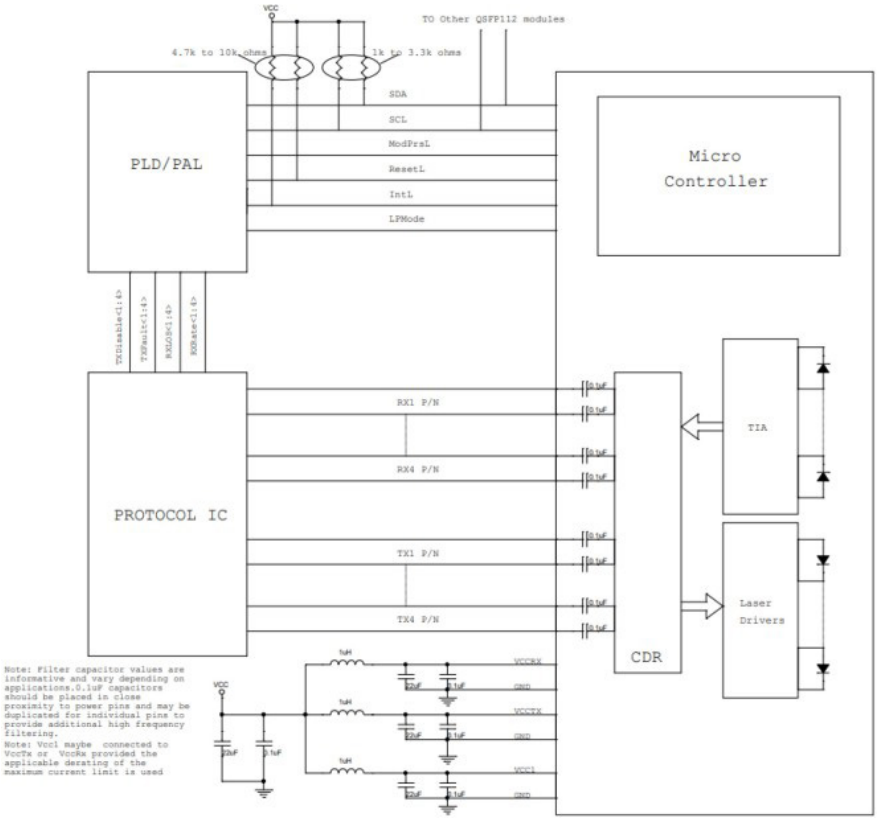

Figure 4

MECHANICAL DIMENSIONS

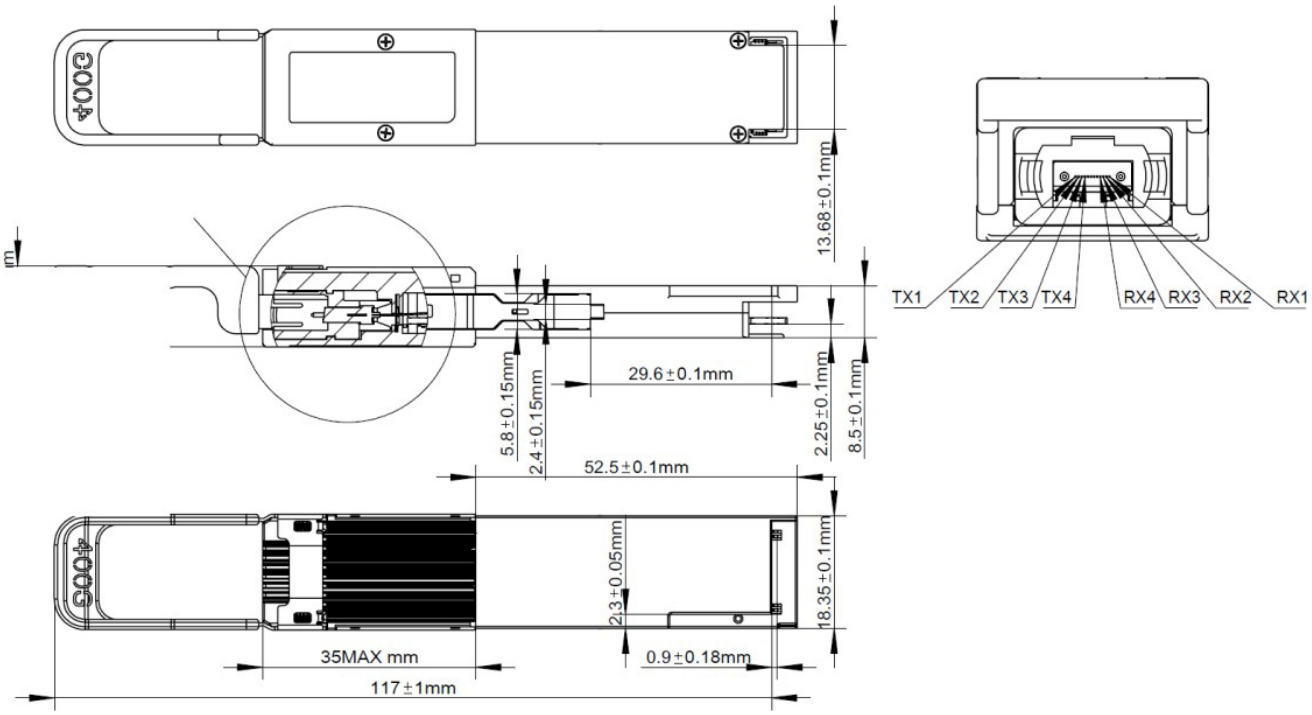

Figure 5

ORDERING INFORMATION

Part Number	Description	Application	Data Rate	Laser Source	Fiber Type
PT-400G-DR4112-31	400G DR4 QSFP112	400GBASE-DR4	400G Ethernet	EML	Single-Mode Fiber