

PT-100G-LR4-31

DATASHEET



1. PRODUCT FEATURES

- ▶ Hot pluggable QSFP28 MSA form factor
- ▶ Compliant to IEEE 802.3ba 100GBASE-LR4
- ▶ Up to 10km reach for G.652 SMF
- ▶ Single +3.3V power supply
- ▶ Operating case temperature: 0~70oC
- ▶ Transmitter: cooled 4x25Gb/s LAN WDM TOSA (1295.56, 1300.05, 1304.58, 1309.14nm)
- ▶ Receiver: 4x25Gb/s PIN ROSA
- ▶ 4x28G Electrical Serial Interface (CEI-28G-VSR)
- ▶ Maximum power consumption 4.0W
- ▶ Duplex LC receptacle
- ▶ RoHS-6 compliant

APPLICATIONS

- ▶ 100GBASE-LR4 Ethernet Links
- ▶ Infiniband QDR and DDR interconnects
- ▶ Client-side 100G Telecom connections

2. GENERAL DESCRIPTION

The PT-100G-LR4-31 is a 100Gb/s transceiver module designed for optical communication applications compliant to 100GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14 nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high performance cooled LAN WDM EA-DFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant to optical interface with IEEE802.3ba Clause 88 100GBASE-LR4 requirements.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

3. FUNCTIONAL DESCRIPTION

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock and Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently, each of 4 EML laser driver IC's converts one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 cooled EML lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches the optical signal in specific wavelength specified in IEEE802.3ba 100GBASE-LR4 requirements. These 4-lane optical signals will be optically multiplexed into a single fiber by a 4-to-1 optical WDM MUX. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or 2-wire serial interface.

The receiver receives 4-lane LAN WDM optical signals. The optical signals are de-multiplexed by a 1-to-4 optical DEMUX and each of the resulting 4 channels of optical signals is fed into one of the 4 receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by the RX portion of the 4-channel CDR. The retimed 4-lane output electrical signals are compliant with IEEE CAUI-4 interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value is reported through the 2-wire serial interface. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL. Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

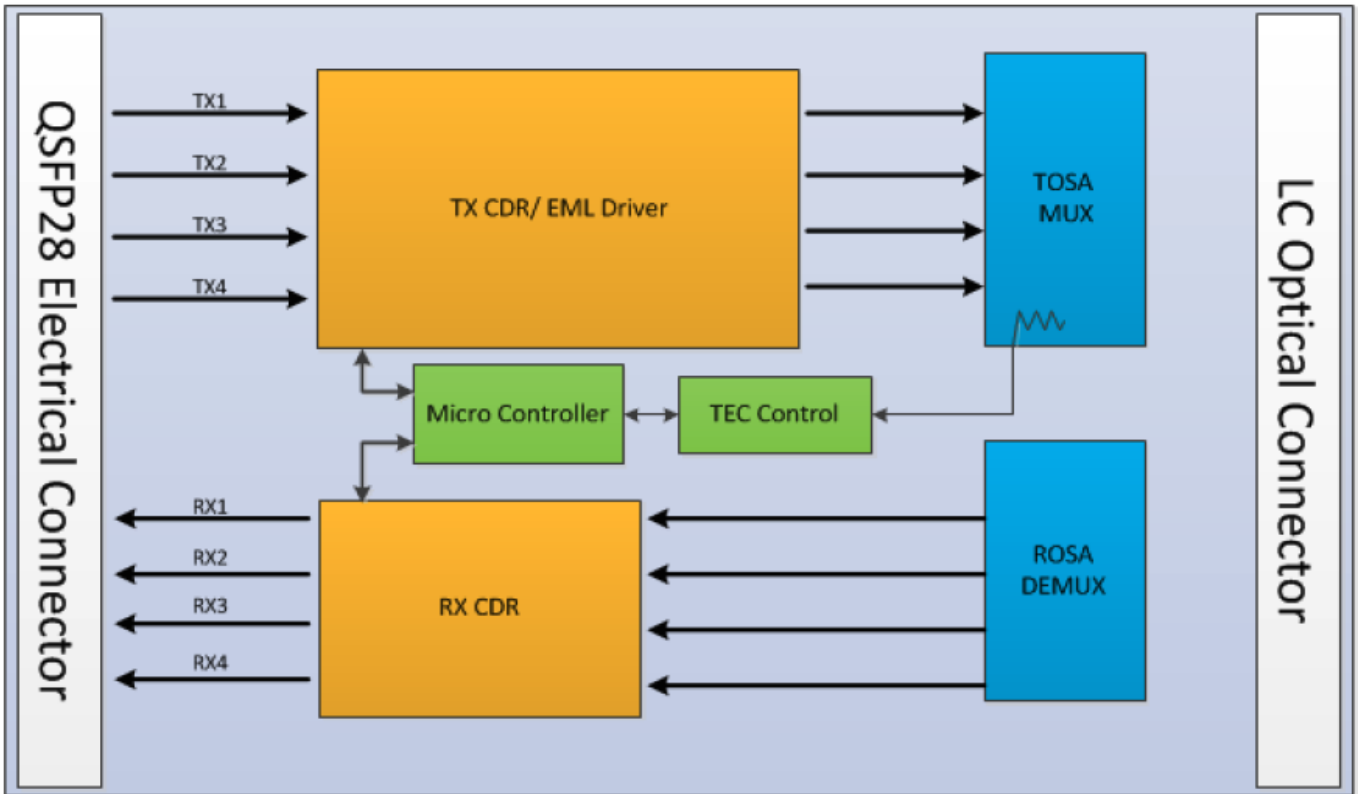
Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset. Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

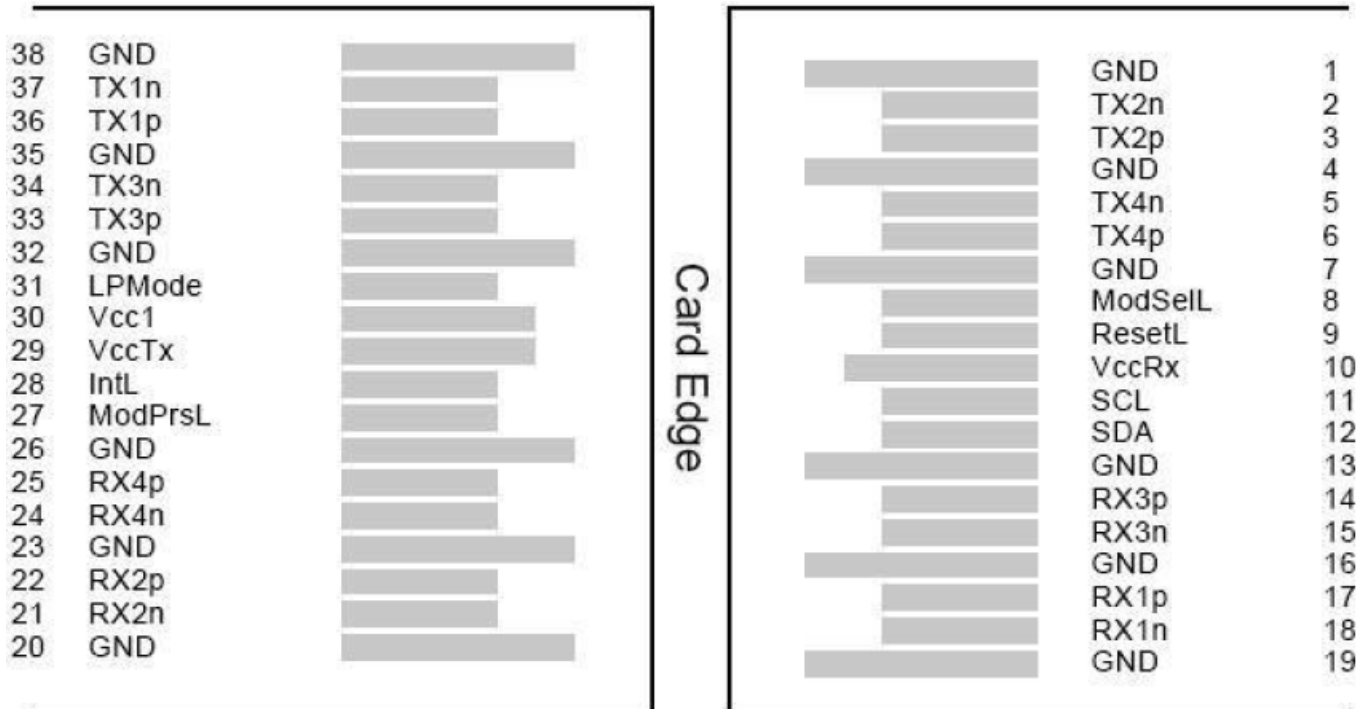
Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

4. TRANSCEIVER BLOCK DIAGRAM



5. PIN ASSIGNMENT AND DESCRIPTION

MSA COMPLIANT CONNECTOR



Top Side viewed from top

Bottom Side viewed from bottom

6. PIN DEFINITION

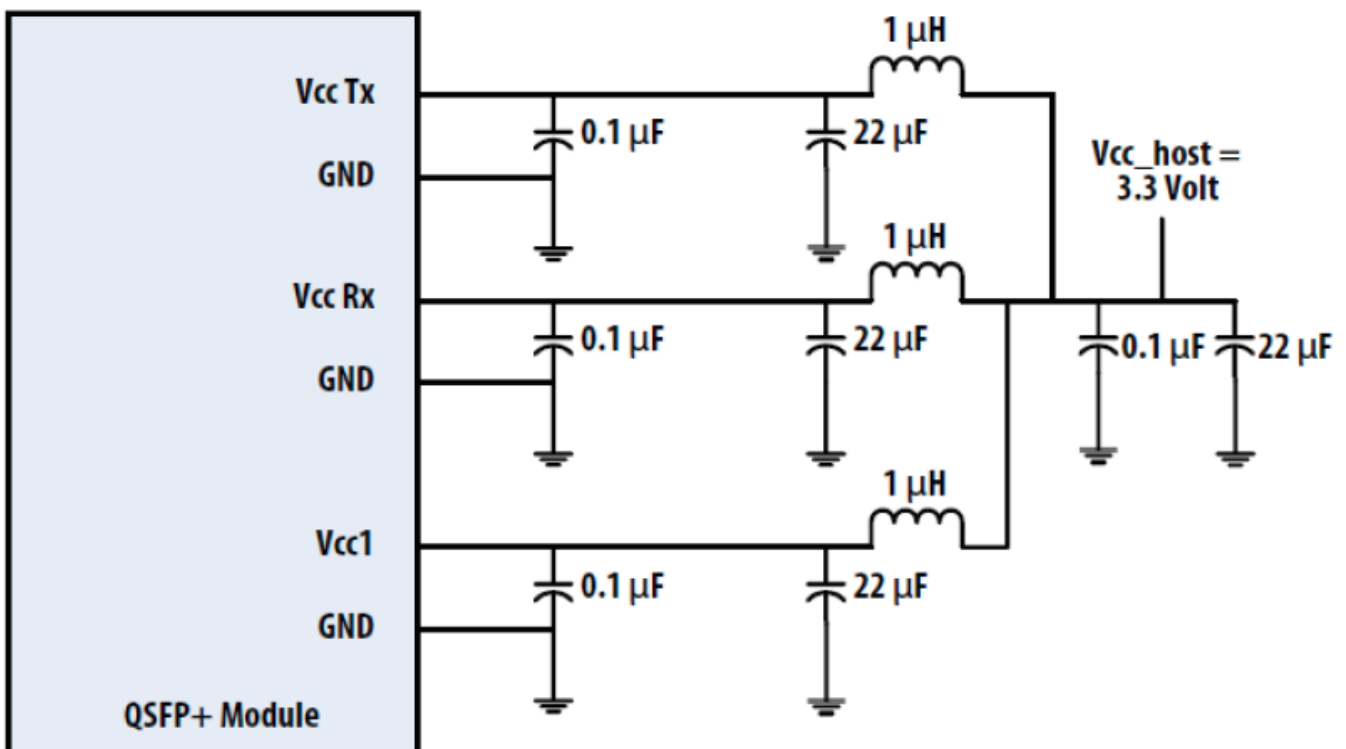
<i>PIN</i>	<i>Logic</i>	<i>Symbol</i>	<i>Name / Description</i>	<i>Note</i>
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTLL-I	ModSelL	Module Select	
9	LVTTLL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3 V Power supply receiver	2
11	LVCNOS-I/O	SCL	2-wire serial interface clock	
12	LVCNOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22		Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTTL-O	ModPrsL	Module Present	
28	LVTTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3 V Power supply transmitter	2
30		Vcc1	+3.3 V Power S	2
31	LVTTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

NOTE

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.

7. RECOMMENDED POWER SUPPLY FILTER



8. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	Ts	-40	85	°C	
Operating Case Temperature	Top	0	70	°C	
Power Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0		%	
Damage Threshold, each Lane	THd	5.5		dBm	

9. RECOMMENDED OPERATING CONDITIONS AND POWER SUPPLY REQUIREMENTS

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	TOP	0		7	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Data Rate, each Lane			25.78125		Gb/s
Control Input Voltage High		2		V	V
Control Input Voltage Low		0		0	V
Link Distance with G.652	D	0.002		1	Km

10. ELECTRICAL CHARACTERISTICS

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential Input Voltage		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	V _{in,pp}	190		700	mVpp	
Differential Input Impedance	Z _{in}	90	10	110	Ohm	

RECEIVER (EACH LANE)

Parameter	Symbol	Min	Typical	Max	Unit	Note
Single-ended Output Voltage		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing	V _{out,pp}	300		850	mVpp	
Differential Input Impedance	Z _{out}	90	10	110	Ohm	

NOTE

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

11. OPTICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Lane Wavelength	L	1294.5	1295.56	1296.59	nm	
	L	1299.0	1300.05	1301.09	nm	
	L	1303.5	1304.58	1305.63	nm	
	L	1308.0	1309.14	1310.19	nm	

TRANSMITTER

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Side Mode Suppression Ratio	SMSR	3			dB	
Total Average Launch Power	PT			10.5	dBm	
Average Launch Power, each Lane	PAVG	-4.3		4.5	dBm	
OMA, each Lane	POMA			4.5	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff	1.3		5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-2.3				
TDP, each Lane	TDP			2.2	dBm	
Extinction Ratio	ER	4			dB	
RIN _{20OMA}	RIN			-130	dB	
Optical Return Loss Tolerance	TOL			20	dB/Hz	
Transmitter Reflectance	RT			-12	dB	
Eye Mask{X1, X2, X3, Y1, Y2, Y3}			{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		dB	2
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	

RECEIVER

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Damage Threshold, each Lane	THd	5			dBm	
Total Average Receive Power				10.5	dBm	
Average Receive Power, each Lane		-10.6		4.5	dBm	
Receive Power (OMA), each Lane				4.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-8.6	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-6.8	dBm	4
Receiver Reflectance	RR			-26	dB	
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			5.5	dB	
LOS Assert	LOSA		-1		dBm	
LOS Deassert	LOSD		-1		dBm	
LOS Hysteresis	LOSH	0			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			31	GHz	

CONDITIONS OF STRESS RECEIVER SENSITIVITY TEST (NOTE 5)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Vertical Eye Closure Penalty, each Lane			1.8		dB	
Stressed Eye J2 Jitter, each Lane			0		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

NOTE

1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. See Figure 4 below.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = 1×10^{-12} .
5. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

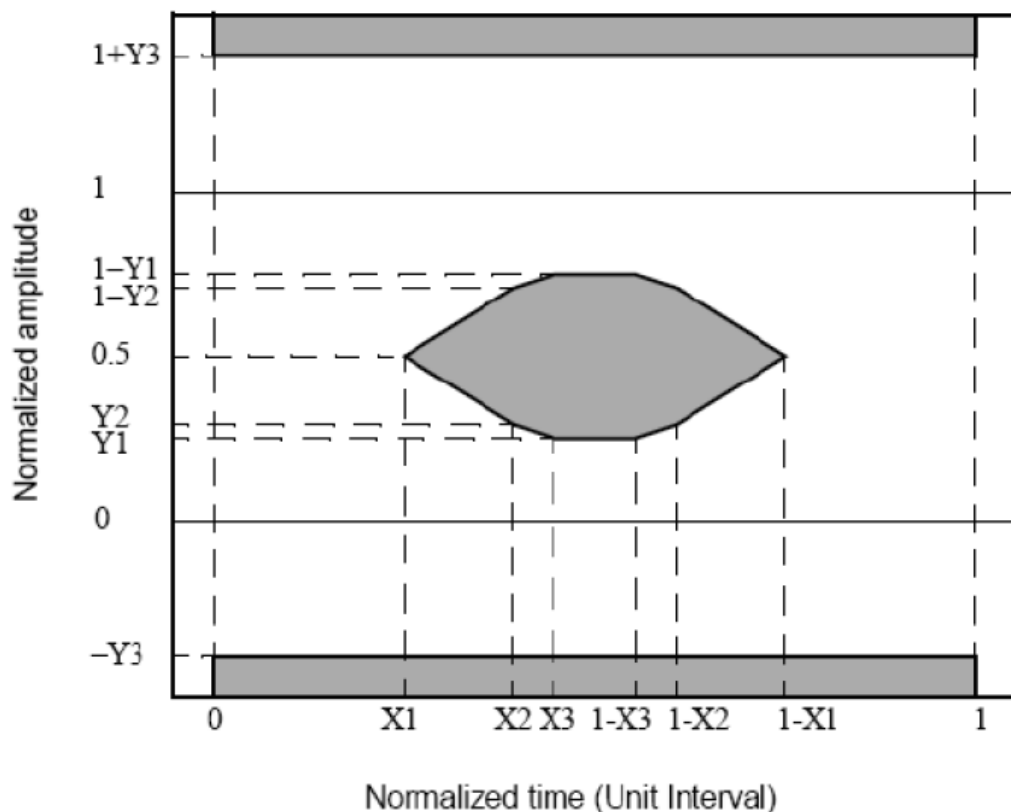


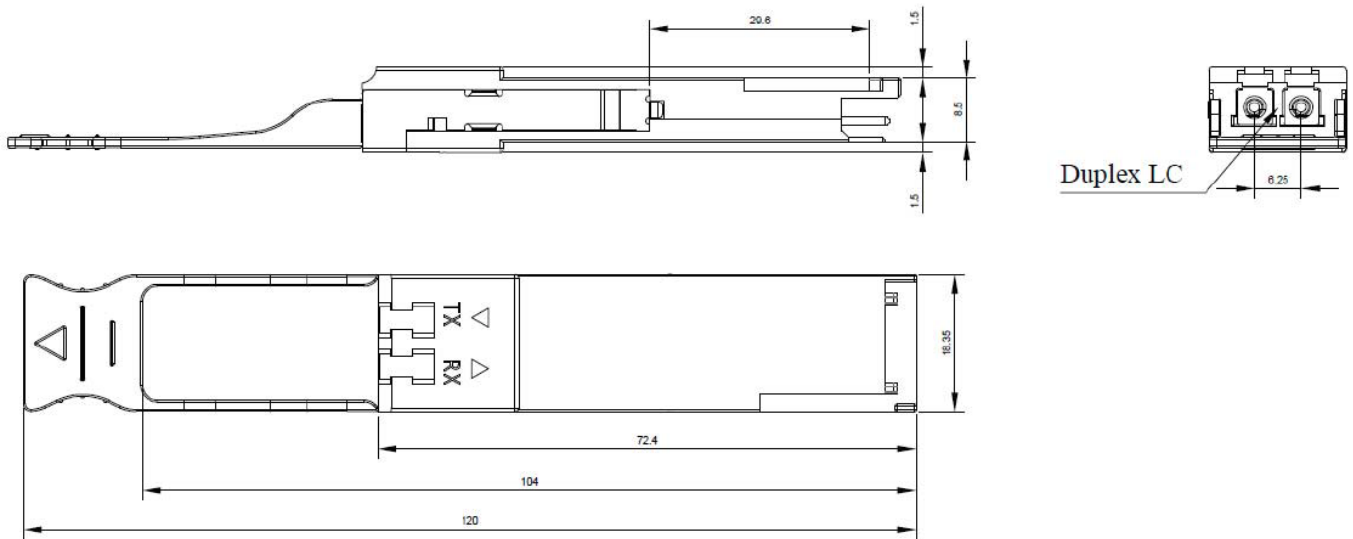
Figure 4. Eye Mask Definition

12. DIGITAL DIAGNOSTIC FUNCTIONS

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3	+3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

13. MECHANICAL DIMENSIONS



14. ESD

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

15. LASER SAFETY

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

16. ORDERING INFORMATION

<i>Part Number</i>	<i>Product Description</i>
PT-100G-LR4-31	100GBASE-LR4 QSFP28 1310NM 10KM

IMPORTANT NOTICE

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Profitap before they become applicable to any particular order or contract. In accordance with the Profitap policy of continuous improvement specifications may change without notice.

The publication of information in this data sheet does not imply freedom from patent or other protective rights of Profitap or others. Further details are available from any Profitap sales representative.